Universidad Zaragoza

Academic Year/course: 2024/25

67236 - FPGA-based digital control for power converters

Syllabus Information

Academic year: 2024/25
Subject: 67236 - FPGA-based digital control for power converters
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 527 - Master's in Electronic Engineering
622 - Master's in Electronic Engineering
ECTS: 6.0
Year: 1
Semester: First semester
Subject type: Optional
Module:

1. General information

This subject studies the implementation techniques of digital control algorithms for power stages in FPGA, using VHDL language and high-level synthesis tools (HLS). For this purpose, it will be necessary to study three fundamental aspects: modulation techniques and their digital implementation to generate the trigger signals of the devices; fixed and floating point implementation of linear regulators; closed-loop simulation techniques of the whole system, including the digital, analogue and power part, to verify the control performance.

2. Learning results

To be able to specify and analyse complex electronic systems with analogue, digital and power blocks.

To be able to conceive and develop advanced digital systems based on programmable devices, configurable logic devices and integrated circuits, with mastery of hardware description tools.

To apply the acquired knowledge to select an FPGA for a given design based on its hardware resources.

To design digital modulators in VHDL for the different power stages.

To design digital linear regulators using fixed-point and floating-point arithmetic with high-level synthesis (HLS) tools.

To know the methodologies based on high-level synthesis tools to implement complex digital designs on FPGA.

To functionally verify the design of the digital control and power stage through closed-loop simulation.

3. Syllabus

- T0. Presentation and introduction to the subject.
- T1. FPGA design for power stages.
- T2. Design review with VHDL.
- T3. Digital generation of trigger signals.
- T4: Design and implementation of digital controllers in HLS.
- T5: VHDL/C simulation of power stages.

There will be 6 sessions of laboratory practices to apply the topics of the subject to real designs.

4. Academic activities

- Participatory master class: 20 hours.
  The contents of the subject will be presented, with a practical orientation towards the design of electronic systems.
- Problem solving and cases: 10 hours.
  Practical design problems will be solved.
- Laboratory practices: 18 hours.
  The integrated digital design environment and FPGA evaluation boards will be used to approach the design and verification of the different blocks studied in the master classes.
- Study and personal work: 96 hours.
- Assessment tests: 6 hours.

5. Assessment system

The subject will be assessed by the continuous assessment system by means of the following activities:

Global exam with theoretical and practical questions (50% of the grade).

A test with questions and problems related to both the theoretical contents and the practices performed will be carried out in the official calls. Subject materials will be available for consult during the exam.

Laboratory practices (50% of the grade).

The work done in the laboratory sessions will be assessed since it is considered that the learning of this subject is associated with practical experimentation. The following aspects will be assessed:

- Previous preparation of the practice.
- Management of electronic design tools.
- Autonomy and participation of each student.
- Design operation on the FPGA.
- Report made at the end of each practice.

The subject is passed with a total grade higher than or equal to 5 points out of 10.

If the student has not passed any of these activities during the semester, they will have the opportunity to pass the subject by means of a global test in the official calls for exams.

6. Sustainable Development Goals

7 - Affordable and Clean Energy
9 - Industry, Innovation and Infrastructure