Universidad Zaragoza

Academic Year/course: 2024/25

30398 - Digital electronics for communications

Syllabus Information

Academic year: 2024/25
Subject: 30398 - Digital electronics for communications
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 581 - Bachelor's Degree in Telecommunications Technology and Services Engineering
ECTS: 6.0
Year: 4
Semester: First semester
Subject type: Optional
Module:

1. General information

The objective of the subject is to train the student in the fundamentals of digital electronic systems design, using HDL language, with special emphasis on arithmetic for signal processing in communications systems.

Not only the basics to implement digital systems efficiently with FPGAs are studied, but it is also intended to achieve analysis and design capabilities.

It is recommended to have taken "Electronic systems with microprocessors", as well as the subjects of digital electronic content of the previous subjects.

These approaches and objectives are aligned with the Sustainable Development Goals (SDGs) of the 2030 Agenda of United Nations (https://www.un.org/sustainabledevelopment/es/), specifically, the learning activities planned in this subject will contribute to the achievement of targets 7.2 and 7.3 of Goal 7, and target 9.4 of Goal 9.

2. Learning results

The student:

Know the design process of an electronic system in its digital part, applying a top-down perspective, from the hierarchical block diagram to the final product.

Will be able to work on an algorithm in the field of control, signal and communications, propose the partitioning of the system and evaluate the best option within the solution space.

Know how to use hardware description languages to model the selected architecture, and select a suitable FPGA based on its technology, internal structure and features. Be experienced in the use of CAD tools from digital design for application to the design of physical and temporal constraints.

Will be able to design in HDL functional validation benches for the designed digital systems, including the verification of the achieved performance, and experimental validation of the designs on commercial development boards.

3. Syllabus

The contents to be developed during the term will include:

1. Design of digital systems and validation environments using HDL.
2. Temporal and physical constraints in digital design.
3. Digital arithmetic, and fixed-point coding with HDL.
4. Architecture and electronic blocks available in the design with FPGAs

4. Academic activities

Lectures: 30 hours

Sessions in which the theoretical contents will be explained. These will be complemented with the development of examples

and problem solving. The time available will be divided in 50% between theoretical presentation and problem solving.

Laboratory practices: 30 hours

Design, and test in FPGA, of small circuits with application to signal processing and communications. CAD tools and design flow will be used to approach the work methodology in the industry.

5. Assessment system

I. Mixed system composed of two assessment activities:

a) Laboratory Practices (30%)

Previous preparatory work, laboratory work, and practice reports with the results of the designs will be graded.

b) Theoretical-practical examination (70%)

Composed of theoretical-practical questions and problems. It is necessary to obtain a minimum score of 4 points out of 10 in this test to pass the subject.

II. Simple system based exclusively on a single overall final assessment test with theoretical-practical questions and design problems.

6. Sustainable Development Goals

7 - Affordable and Clean Energy
9 - Industry, Innovation and Infrastructure