Universidad Zaragoza

Academic Year/course: 2023/24

39822 - Computer architecture and organisation II

Syllabus Information

Academic year: 2023/24
Subject: 39822 - Computer architecture and organisation II
Faculty / School: 326 - Escuela Universitaria Politécnica de Teruel
Degree: 634 - Joint Programme in Computer Engineering - Business Administration
ECTS: 6.0
Year: 2
Semester: Second semester
Subject type: Compulsory
Module:

1. General information

This subject completes the essential knowledge in Computer Engineering related to the organization and architecture of computers, which began to be introduced in Introduction to Computers, Architecture and Organization of Computers 1 and Operating Systems. Its objectives are:

- To present the basic models of computer performance evaluation.
- To introduce the organization and operation of a basic processor-memory-peripheral system, so that efficient programming can be carried out.
- Improve logic design skills to be able to tackle larger problems such as the design of a simple processor or an input/output interface.

Computer engineering is a cross-cutting discipline that can be applied to help meet all the challenges of the Sustainable Development Goals, SDGs, of Agenda 2030 (https://www.un.org/sustainabledevelopment/es/).

2. Learning results

Understand the importance of performance measurement in the computer world and how it is performed.

Understand segmentation, its benefits, problems and basic solution methods.

Understand the usefulness of the memory hierarchy and the principles on which it is based.

Understandsthe operation of a cached memory system.

Understand the operation and usefulness of the buses.

Know the characteristics of some typical input/output devices.

Be able to use the above knowledge to design a simple processor, cache memory, bus or input/output interface.

3. Syllabus

- Design of a complex digital system.
- Introduction to performance analysis.
- Processor organization: non-segmented machines. Exceptions and processor modes. Segmentation.
- Memory system: types of memory, locality principle and memory hierarchy, cache memories, organization of main memory.
- Buses and input/output devices.

4. Academic activities

- Attendance with profit in the face-to-face classes

- 2 h / week

- Problem solving in small groups

  - 1 h / week

- Performance of laboratory-assisted practices

  - 1 h / week

- Personal study and work, for which, in addition to the material used in classes and the laboratory, a collection of problems is provided and practical projects supervised by the faculty are proposed[J5]. Resolution of doubts through personalized tutorials or in small groups (85 hours estimated)

- Completion of the corresponding evaluation tests (5 hours)

5. Assessment system

This global assessment test will take place on the dates established by each center. The timetable for the tests will be defined by the teaching staff of the subject well in advance.

1. Final written test that will include conceptual questions, problems, as well as aspects related to the practices (75% of the final grade).

2. Academic work during the practice or practrical exam (25% of the final grade).

A score of 4 out of 10 in each section is required for averaging.