Universidad Zaragoza

Academic Year/course: 2023/24

30235 - Commercial Processors

Syllabus Information

Academic year: 2023/24
Subject: 30235 - Commercial Processors
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 439 - Bachelor's Degree in Informatics Engineering
ECTS: 6.0
Year: 3
Semester: Second semester
Subject type:
Module:

1. General information

This subject continues the line started with the subjects "Architecture and Organization I and II", seeking to increase and deepen the theoretical and practical knowledge about computer organization, processor architecture and its relationship with the compiler.

The course ends with examples of the main architectures on the market, which will allow us to: i) obtain efficient codes (in terms of resources, time or consumption) for all of them, ii) analyze, evaluate and select the most suitable hardware platforms for different fields, (iii) to develop new processors adapted to specific needs.

This is a subject whose evaluable contents alone do not yet give the student direct capabilities to contribute to the achievement of the SDGs.

To take this subject it is recommended to have taken the course Computer Architecture and Organization 2.

2. Learning results

Know performance enhancement techniques, such as multithreading and out-of-order execution, and knows how to analyze their influence on system performance.

Know the architectures of contemporary general purpose processors, identifying their objectives (cost, speed, power consumption, etc.). Be capable of improving the performance of target-critical code, manually or by guiding the compiler through the compilation options.

Know repertoire extensions (multimedia, security, etc.) and the role of the compiler in their exploitation (vectorization, iterative compilation, etc.).

Know various specific-purpose architectures, such as microcontrollers, DSPs, multimedia processors, graphics processors, or network processors.

3. Syllabus

Introduction

Module 1: Processor organization

- Segmented review: exception handling
- Multicycle operations. Execution out of order
- Register and memory renaming. Prediction of jumps
- Multithreading

Module 2: Organization of the memory hierarchy

- Review: basic performance enhancement techniques
- Advanced performance enhancement techniques
- Segmented access to caches
- Multiport Caches

- Non-blocking caches
- Pre-search

Module 3: Machine language architecture Design options

- RISC example: ARM
- Example CISC: Intel
- Example VLIW: DSP TMS

Module 4: Compilation

- Compilation stages
- Register assignment and instruction scheduling
- Optimization
- Hierarchy-oriented code optimization

4. Academic activities

- Lectures: the main aspects of each concept will be presented.
- Problem solving classes: problems related to the syllabus will be solved. These classes will be interspersed with the lectures.
- Assisted laboratory practice: the main components of a high performance processor will be implemented in a simulator.
- Study and personal work.
- Completion of the corresponding evaluation tests

5. Assessment system

The assessment will consist of three parts:

1. Defense of the laboratory practicals (30 points).
2. Presentation of results on practical work (10 points).
3. Theory and problems exam (60 points).

To pass the subject you must obtain at least 50 points out of the total and at least 24 points out of 60, that is, a 4 out of 10, in the exam. In the case of not achieving a 4 out of 10 in the exam, the grade in the call will coincide with the obtained in the exam.

An added section may be requested in the examination to replace the marks for parts 1 and 2.