Universidad Zaragoza

Academic Year/course: 2021/22

67236 - FPGA-based digital control for power converters

Syllabus Information

Academic Year: 2021/22
Subject: 67236 - Control digital con FPGA de etapas de potencia
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 527 - Master's in Electronic Engineering
622 - Master's in Electronic Engineering
ECTS: 6.0
Year: 1
Semester: 622 - First semester
527 - Second semester
Subject Type: Optional
Module:

1. General information

2. Learning goals

3. Assessment (1st and 2nd call)

3.1. Assessment tasks (description of tasks, marking system and assessment criteria)

The final grade for this course is based on the following weighting:

- Final exam (50 % of grade)
- Pre-lab work, attendance, attitude, and accomplishment during laboratory session (30 %)
- Guided assignment and laboratory reports (20 %)

4. Methodology, learning tasks, syllabus and resources

4.1. Methodological overview

The methodology followed in this course is oriented towards achievement of the learning objectives. It is based on participation and the active role of the student that favor the development of communication and decision-making skills. A wide range of teaching and learning tasks are implemented, such as lectures, guided assignments, laboratory sessions, autonomous work, and tutorials.

Students are expected to participate actively in the class throughout the semester.

Classroom materials will be available via Moodle. These include a repository of the lecture notes used in class, the course syllabus, as well as other course-specific learning materials.

Further information regarding the course will be provided on the first day of class.

4.2. Learning tasks

The course includes 6 ECTS organized according to:

- Lectures (20 hours). Explanation of theoretical contents.
- Practice sessions (10 hours). Problem-solving and case studies.
- Laboratory sessions (18 hours).

- Assignments and homework (40 hours).
- Autonomous work and study (59 hours).
- Final exam (3 hours).

4.3. Syllabus

The course will address the following topics:

- Topic 1. Design with FPGA for switched-mode power electronic converters.
- Topic 2. Arithmetic and VHDL coding.
- Topic 3. VHDL modeling of switched-mode power electronic converters for test bench generation.
- Topic 4. FPGA-based gate signal generation for power electronic converters.
- Topic 5. Implementation of digital controllers for power electronic converters using high level synthesis tools.

6 laboratory sessions will be carried out to apply the lecture topics in real designs.

4.4. Course planning and calendar

Laboratory sessions will take place every 2 weeks (6 sessions in total) and last 3 hours each.

Further information concerning the timetable, classroom, office hours, assessment dates and other details regarding this course, will be provided on the first day of class or please refer to the EINA website (https://eina.unizar.es).

4.5. Bibliography and recommended resources

Basic bibliography could be found in the library website:

http://psfunizar10.unizar.es/br13/egAsignaturas.php?codigo=60837