Universidad Zaragoza

Academic Year/course: 2021/22

30315 - Digital Electronics

Syllabus Information

Academic Year: 2021/22
Subject: 30315 - Digital Electronics
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 438 - Bachelor's Degree in Telecomunications Technology and Services Engineering
581 - Bachelor's Degree in Telecomunications Technology and Services Engineering
ECTS: 6.0
Year: 2
Semester: Second semester
Subject Type: Compulsory
Module:

1. General information

2. Learning goals

3. Assessment (1st and 2nd call)

4. Methodology, learning tasks, syllabus and resources

4.1. Methodological overview

The process of teaching and learning designed for this subject is based on the following. It will involve two different training activities with increasing student participation as the course progresses: lectures and laboratory sessions.

- Face-to-face sessions will have an eminently practical orientation. In the more theoretical lectures, the basis of digital systems design will be presented, setting out the fundamental aspects. 1/3rd of these sessions will be dedicated to solving and discussing design problems.
- The second training activity will focus on the laboratory sessions in small groups, where the students will work with design CAD tools.

4.2. Learning tasks

The program, offered to the students to achieve the learning goals, includes the following activities:

Lectures (A01) and exercises and cases solving (A02):

In this activity, the fundamental contents of the subject will be presented, with a practical orientation based on the digital systems design. This activity will take place in person. The necessary materials will be available to students through the ADD.

Laboratory sessions (A03):

This activity is structured in 6 practical sessions of 2.5 hours each. The scripts will be available to students in the ADD well in advance. In these sessions, the required CAD tools for digital electronic design will be used, so that students will acquire the skills and abilities necessary to address digital design.

Evaluation tests (A08): Evaluation activity includes performing a global test.

Study (T7):

This activity includes personal work aimed at achieving the adequate pursuit of the subject, conducting lab sessions and the tutoring process.

4.3. Syllabus

The course will address the following topics:

UNIT 1. Digital design in PLDs using VHDL.

1: Hardware Implementation of Logical Systems.

- Implementation options
- Introduction to Programmable Logic Devices (PLDs). FPGAs
- Hardware description language VHDL
    - Core items
    - Objects, classes and types
    - Operators
    - Structure of a VHDL file
        - Entity
        - Architecture
    - Sentences
    - Concurrent and sequential statements
    - Modeling styles
    - Simulation
    - Test environments
    - Design of digital electronic systems
    - Methodology, tools and design flow

2: VHDL Modeling of digital systems.

- Combinational Systems
    - Code converters
    - Decoders and encoders
    - Information distributors
    - Multiplexers and demultiplexers
    - Tristate adapters
    - Generators / Parity testers
    - Arithmetic operators
    - Arithmetic Packages in VHDL
    - Comparators of magnitude
    - Summers and subtractors
    - Multipliers
    - Look-up table (ROM)
- Sequential systems
    - Bistables
    - Registers
    - Counters
- Digital circuit design rules
    - Description VHDL oriented to HW

3: RTL design.

- RTL architecture
    - Control
        - State machines (FSM)
    - I/O Interfaces
        - AXI4-Stream
    - Data Path
        - Sequential iterative circuit
- Design examples:

        - Signal processing FIR filter
        - Interface. A / D converter control ADC7476
        - ...
- Functional verification.

UNIT 2. Technologies of the C.I. Digital

4: Technologies of digital circuits.

- Device technology CMOS technology
- Special Input/Output structures
    - Open drain(collector) outputs
      Tristate departures
      Schmitt-trigger tickets
      Generation of the clock
      Operational characteristics and basic parameters of c.i. digital
      Interconnection
      Implementation technologies
      Fixed function integrated circuits
      Programmable logic devices (SPLD, CPLD and FPGA)

Labs:

- **Introduction to design tools.** Fire alarm system.
- **Combinational systems.** 7 segment display.
- **Sequential systems.** Asynchronous serial transmission.
- **Finite State Machines.** Asynchronous serial reception.
- **Numbering systems.** Digital oscillator with AXI4-Stream Interface.
- **Design exercise.**

  (*the concrete exercises/designs in each lab can be modified*)

4.4. Course planning and calendar

Both theoretical classes and laboratory sessions are held according to the schedule set by the center (available on the corresponding website). The other activities will be planned depending on the number of students and will be announced well in advance.

Each teacher will inform of the particular tutoring hours.

4.5. Bibliography and recommended resources

1. Basic teaching materials. Available in http://add.unizar.es (To access this resource, the student must be enrolled in the subject).

- **Slides.** They are considered the notes of the subject.
- **Practices scripts.**
- **Supplementary teaching materials.** Set of useful materials for the course: catalogs of manufacturers, component data sheets, CAD tools, manuals, etc.

2. Reference and complementary books

http://psfunizar10.unizar.es/br13/egAsignaturas.php?codigo=30315