Universidad Zaragoza

Year : 2019/20

60837 - FPGA-Based Digital Control for Power Converters

Syllabus Information

Academic Year: 2019/20
Subject: 60837 - FPGA-Based Digital Control for Power Converters
Faculty / School: 110 -

Degree: 532 - Master's in Industrial Engineering

ECTS: 6.0
Year: 2
Semester: First semester
Subject Type: Optional
Module: ---

1.General information

1.1.Aims of the course

1.2.Context and importance of this course in the degree

1.3.Recommendations to take this course

2.Learning goals

2.1.Competences

2.2.Learning goals

2.3.Importance of learning goals

3.Assessment (1st and 2nd call)

3.1.Assessment tasks (description of tasks, marking system and assessment criteria)

Course grading
The final grade for this course is based on the following weighting:
- Final exam (50 % of grade)
- Pre-lab work, attendance, attitude, and accomplishment during laboratory sessions (30 %)
- Laboratory reports (20 %)

4.Methodology, learning tasks, syllabus and resources

4.1.Methodological overview

The methodology followed in this course is oriented towards achievement of the learning objectives. A wide range of teaching and learning tasks are implemented, such as

- Lectures, where the theoretical concepts of the design of FPGA-based digital electronic systems for power electronic applications will be presented, illustrated with numerous examples.
- Several sessions will be devoted to apply the theoretical concepts to solve problems and case studies.
- Laboratory sessions will be conducted in small groups where students simulate, program and check the operation of the FPGA-based digital electronic systems.

4.2.Learning tasks

The course includes the following learning tasks:

- Lectures (20 hours). Explanation of theoretical contents.
- Practice sessions (10 hours). Problem solving and case studies.
- Laboratory sessions (18 hours). 6 sessions of 3 hours each.
- Assignments and homework (35 hours).
- Tutorials for assignment supervision (5 hours).
- Autonomous work and study (60 hours).
- Final exam (2 hours).

4.3.Syllabus

The course will address the following topics:

Lectures

- Topic 1. Design with FPGA for switched-mode power electronic converters.
- Topic 2. Arithmetic and VHDL coding.
- Topic 3. VHDL modeling of switched-mode power converters for test bench generation.
- Topic 4. FPGA-based gate signal generation for power electronic converters.
- Topic 5. VHDL description of digital controllers for power electronic converters.

Laboratory sessions

- Session 1. FPGA interface to a 1-wire temperature sensor. Simulation + practical work.
- Session 2. FPGA interface with an A / D converter. Simulation + practical work.
- Session 3. VHDL Modeling of a Buck converter. Simulation.
- Session 4. FPGA-Based Sigma-delta modulator. Simulation + practical work.
- Session 5. Digital Control of a Buck Converter I. Simulation.
- Session 6. Digital Control of a Buck Converter II. Simulation + practical work.

4.4.Course planning and calendar

Further information concerning the timetable, classroom, office hours, assessment dates and other details regarding this course, will be provided on the first day of class or please refer to the EINA website (http://eina.unizar.es).

4.5.Bibliography and recommended resources

Basic bibliography could be found in the library website.