Universidad Zaragoza

Year : 2019/20

30235 - Commercial Processors

Syllabus Information

Academic Year: 2019/20
Subject: 30235 - Commercial Processors
Faculty / School: 110 - Escuela de Ingeniería y Arquitectura
Degree: 439 - Bachelor's Degree in Informatics Engineering
ECTS: 6.0
Year: 3
Semester: Second semester
Subject Type: ---
Module: ---

1.General information

1.1.Aims of the course

1.2.Context and importance of this course in the degree

1.3.Recommendations to take this course

2.Learning goals

2.1.Competences

2.2.Learning goals

2.3.Importance of learning goals

3.Assessment (1st and 2nd call)

3.1.Assessment tasks (description of tasks, marking system and assessment criteria)

4.Methodology, learning tasks, syllabus and resources

4.1.Methodological overview

The methodology followed in this course is oriented towards the achievement of the learning objectives. A wide range of teaching and learning tasks are implemented.

4.2.Learning tasks

The program offered to help the student achieve the expected results includes the following activities:
- Class attendance
- Problem solving in small groups
- Performing assisted laboratory practices .
- Study and personal work, for which, in addition to the material used in the classroom and the laboratory
- Resolution of doubts through personal tutorials or in small groups
- Accomplishment of the corresponding evaluation tests

4.3.Syllabus

The course will address the following topics:

Introduction

Topic 1: Processor organization

Review of Segmentation: exception Handling
Multicycle operations. Out of order execution.
Register renaming and memory disambiguation.

Branch prediction
Multithreading

Topic 2: Memory hierarchy organization
Review: basic techniques for improving performance
Advanced techniques for improving performance
Segmented cache access
Multi ported caches
Non-blocking caches
Prefetching

Topic 3: Instruction set architecture
Design Options
RISC example: general purpose SPARC
CISC example: general purpose Intel
VLIW example: DSP TMS

Topic 4: Compilation
Stages of compilation
Register allocation and instruction scheduling
Optimization
Memory hierarchy oriented code optimization

4.4.Course planning and calendar

The course is organized in 2 hours of class and 1 hour of problems each week.

In addition, 6 sessions of practice of 2 hours each are performed.

The schedule will be implemented for each teaching group when the academic calendar of the University of Zaragoza is approved

4.5.Bibliography and recommended resources

[BB: Bibliografía básica / BC: Bibliografía complementaria]

http://psfunizar7.unizar.es/br13/egAsignaturas.php?codigo=30235&Identificador=14700

- [BB] Baer, Jean-Loup. Microprocessor architecture : from simple pipelines to chip multiprocessor / Jean-Loup Baer . New York : Cambridge University Press, 2010
- [BB] González Colás, Antonio. Processor microarchitecture : an implementation perspective / Antonio González, Fernando Latorre and Grigorios Magklis . San Rafael : Morgan & Claypool, cop. 2011
- [BB] Hennessy, John L. Computer architecture : a quantitative approach / John Hennessy, David A. Patterson ; with contributions by Andrea C. Arpaci-Dusseau ... [et al.] . 4th ed. San Francisco : Morgan Kaufmann, 2007
- [BB] Patterson, David A.. Estructura y diseño de computadores : la interfaz software/hardware / David A. Patterson, John L. Hennessy ; con contribuciones de Perry Alexander ... [et al. ; versión española por, Javier Díaz Bruguera] Barcelona : Reverté, D.L. 2011