Universidad Zaragoza
1542

Year : 2018/19

30235 - Commercial Processors

Syllabus Information

Academic Year:	2018/19
Subject:	30235 - Commercial Processors
Faculty / School:	110 -
Degree:	439 - Bachelor's Degree in Informatics Engineering
ECTS:	6.0
Year:	3
Semester:	Indeterminate
Subject Type:	
Module:	---

General information

Aims of the course

Context and importance of this course in the degree

Recommendations to take this course

Learning goals

Competences

Learning goals

Importance of learning goals

Assessment (1st and 2nd call)

Assessment tasks (description of tasks, marking system and assessment criteria)

Methodology, learning tasks, syllabus and resources

Methodological overview

Monitoring of learning activities for this subject.

Learning tasks

The program offered to help the student achieve the expected results includes the following activities:
- Class attendance
- Problem solving in small groups
- Performing assisted laboratory practices .
- Study and personal work, for which, in addition to the material used in the classroom and the laboratory
- Resolution of doubts through personal tutorials or in small groups
- Accomplishment of the corresponding evaluation tests

Syllabus

Introduction
Module 1: Processor organization
Review of Segmentation: exception Handling
Multicycle operations. Out of order execution.
Register renaming and memory dissambiguation.

Branch prediction
Multithreading
Module 2: Memory hierarchy organization
Review: basic techniques for improving performance
Advanced techniques for improving performance
Segmented cache access
Multiported caches
Non-blocking caches
Prefetching
Module 3: Instruction set architecture
Design Options
RISC example: general purpose SPARC
CISC example: general purpose Intel
VLIW example: DSP TMS
Module 4: Compilation
Stages of compilation
Register allocation and instruction scheduling
Optimization
Memory hierarchy oriented code optimization

Course planning and calendar

The course is organized in 2 hours of class and 1 hour of problems each week.
In addition, 6 sessions of practice of 2 hours each are performed.
The schedule will be implemented for each teaching group when the academic calendar of the University of Zaragoza is approved

Bibliography and recommended resources

[BB: Bibliografía básica / BC: Bibliografía complementaria]

- [BB] Baer, Jean-Loup. Microprocessor architecture : from simple pipelines to chip multiprocessor / Jean-Loup Baer . New York : Cambridge University Press, 2010
- [BB] González Colás, Antonio. Processor microarchitecture : an implementation perspective / Antonio González, Fernando Latorre and Grigorios Magklis . San Rafael : Morgan & Claypool, cop. 2011
- [BB] Hennessy, John L. Computer architecture : a quantitative approach / John Hennessy, David A. Patterson ; with contributions by Andrea C. Arpaci-Dusseau ... [et al.] . 4th ed. San Francisco : Morgan Kaufmann, 2007
- [BB] Patterson, David A.. Estructura y diseño de computadores : la interfaz software/hardware / David A. Patterson, John L. Hennessy ; con contribuciones de Perry Alexander ... [et al. ; versión española por, Javier Díaz Bruguera] Barcelona : Reverté, D.L. 2011