29852 - Digital Design and Control with FPGA

Información del Plan Docente

Academic Year	2018/19
Subject	29852 - Digital Design and Control with FPGA
Faculty / School	110 - Escuela de Ingeniería y Arquitectura
Degree	440 - Bachelor's Degree in Electronic and Automatic Engineering
ECTS	6.0
Year	4
Semester	First semester
Subject Type	Optional
Module	---

1.General information

1.1.Aims of the course

1.2.Context and importance of this course in the degree

1.3.Recommendations to take this course

2.Learning goals

2.1.Competences

2.2.Learning goals

2.3.Importance of learning goals

3.Assessment (1st and 2nd call)

3.1.Assessment tasks (description of tasks, marking system and assessment criteria)

The final grade for this course is based on the following weighting:

- Final exam (50 % of grade)
- Laboratory work, attendance, attitude, accomplishment during laboratory session , and reports (50 %)

4.Methodology, learning tasks, syllabus and resources

4.1.Methodological overview

The methodology followed in this course is oriented towards achievement of the learning objectives. It is based on participation and the active role of the student that favor the development of communication and decision-making skills. A wide range of teaching and learning tasks are implemented, such as lectures, guided assignments, laboratory sessions, autonomous work, and tutorials.

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Students are expected to participate actively in the class throughout the semester.

Classroom materials will be available via Moodle. These include a repository of the lecture notes used in class, the course syllabus, as well as other course-specific learning materials.

Further information regarding the course will be provided on the first day of class.

4.2.Learning tasks

The course includes 6 ECTS corresponding to 150 hour of student work, organized according to:

- Lectures (30 hours).
- Laboratory sessions (30 hours).
- Guided assignments (38 hours).
- Autonomous work (50 hours).
- Assessment (2 hours).

4.3.Syllabus

The course will address the following topics:

Lectures

- Topic 1. Advanced concepts in VHDL
- Topic 2. Arithmetic operations in VHDL
- Topic 3. FPGA implementation of LTI discrete systems
- Topic 4. FPGA arquitecture
- Topic 5. Advanced digital design

Laboratory sessions

- Asynchronous serial receiver
- Asynchronous serial transmitter
- Sinusoidal oscillator
- VGA display controller
- Digital control of a Buck Converter
    - ADC interface
    - Test bench and controller with real type
    - Fixed point controller

Moreover, last 3 laboratory sessions will be dedicated to develop a free design that contains some of the circuit blocks introduced in the course: IP cores, LTI systems, or FPGA board peripherals.

4.4.Course planning and calendar

Lectures run for 2 weekly hours. Laboratory sessions will take place every week (10 sessions in total) and last 3 hours each.

Further information concerning the timetable, classroom, office hours, assessment dates and other details regarding this course, will be provided on the first day of class or please refer to the EINA website (eina.unizar.es).

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4.5.Bibliography and recommended resources